Remarks

Claim Rejections – 35 USC 102

Claim 1:

It is respectfully submitted that Paniccia does not disclose a method of testing the ESD performance of an integrated circuit (IC).

The present application describes and claims a new method of testing the resilience of an IC device to electrostatic discharge (ESD). ESD is described in the Description of the Prior Art section of the present application, and mentions the importance of determining the resilience of an IC device to ESD. For instance, as discussed, prior art methods of testing resilience to ESD events involve discharging charge into the IC pins (page 1, lines 11-16). In contrast, the present invention provides a way of determining ESD resilience in a non-destructive manner using a laser beam, and making a determination based on the amount of light reflected by the diffusion region of the IC compared to the amount of light absorbed by the diffusion region. This has nothing to do with debugging a chip to determine whether it has defects. In fact the chip may very well work fine but have a low ability to handle electrostatic discharge. It is this ability to handle ESD that the present invention addresses, and manages to do in a non-destructive manner.

Paniccia, on the other hand, deals with debugging of semiconductor devices, especially C4 or flip chip devices. This purpose is made clear in the Description of the Related Art section of Paniccia. Thus Paniccia is providing a solution for determining defects in a semiconductor device. In order to achieve this purpose, Paniccia looks at junction voltages by monitoring modulations in the reflected light. As stated on column 6, lines 33-37, "The modulation of the photo-absorption of the laser beam 609 depends on the modulation of the electric field applied at the junction. This modulation in the absorption of the laser beam is the signal of interest since it is related to the voltage applied to the junction."

Nowhere does Paniccia disclose or even suggest a method of testing ESD performance of an IC device. The examiner is respectfully requested to point out where Paniccia makes any reference to testing ESD resilience of an IC device. Furthermore, Paniccia does not even suggest providing a solution to the problem addressed by the present invention, and can therefore not even serve as a section 103 reference. Paniccia deals with an entirely different problem, namely debugging a packaged IC without having to mill away portions of the IC in order to establish an electric contact. As discussed in column 7, lines 18-23, the electro-absorption characteristics in silicon are used to provide information about the electric field and thus the voltage applied to the P-N junction. Thus the measurements taken by Paniccia serve a specific purpose and do not provide any information about ESD resilience or suggest that it could provide information about ESD resilience.

Dependent Claims:

All of the other claims are dependent from claim 1, and therefore include all of the limitations of claim1, which specifies a method of testing the ESD performance of an IC device. All of the claims are, therefore, distinguishable over Paniccia.

Furthermore, as to claim 8, it is respectfully submitted that Paniccia does not disclose taking several samples of each probed location and averaging the results. In fact Figure 7 and column 7, lines 1-27 deal with measurements taken under different conditions (different temperature and wavelength) and show how absorption varies. Paniccia does not discuss taking several samples of one location under the same conditions and averaging the results. In fact, Paniccia teaches away from doing so since it specifically uses different parameters to provide different results, which don't lend themselves to being averaged (it only makes sense to average results if there are several results taken under the same conditions).

In contrast, the present invention contemplates taking several samples under the same conditions to provide an average. For instance, page 4, lines 16-18 discusses sampling the same location 100 times under the same voltage levels to give a reading such as the peak 318 in Figure 3.

Furthermore, as to claims 10 and 18, Paniccia does not disclose using a continuous laser to position the mode-locked laser. In fact column 8, lines 6-15 does not even mention a continuous laser, but specifically mentions only a mode-locked laser (column 8, line 8).

Furthermore, as to claims 14-15, Paniccia does not disclose testing a device in pre-packaged form. Column 1, lines 50-55, cited by the Examiner, in fact specifically discusses the challenges of testing a packaged device that is packaged into C4. It is for this reason that Paniccia suggests probing through the back of the packaged device (column 2, lines 5-12). Thus Paniccia specifically seeks to provide a solution for testing a packaged device.

Furthermore, as to claim 16, Paniccia does not disclose testing a device having only some of its layers. In fact, the cited section (column 1, lines 63-65) simply discusses one prior art approach of probing through the front end – it does not discuss or even suggest probing prior to completion of all layers. In fact it states the difficulty of probing multiple layer devices and the need to expose nodes for probing by subsequently milling away the dielectric or metal. Thus it teaches away from testing the device prior to completion of all the layers.

Accordingly, it is respectfully submitted that all of the claims are distinguishable over Paniccia and are therefore in a position for allowance. The Examiner is, therefore, respectfully requested to allow the application with claims 1-20 to proceed to allowance.

Respectfully Submitted,

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